What is claimed is:

1. A method of forming a gate structure of a semiconductor device, comprising:

forming a first insulating layer on a substrate, subsequently coating the substrate with a conductive material, and patterning the conductive material to form at least one gate pattern insulated from the substrate by the first insulating layer;

forming a second insulating layer on the gate pattern and the substrate;

removing some of the second insulating layer until an upper surface thereof is below a level of an upper surface of the gate pattern;

forming a second conductive layer comprising the conductive material on the second insulating layer and the gate pattern;

selectively removing portions of the second conductive layer such that the second insulating layer is exposed, so that a spacer of the conductive material is formed at both sides of an upper portion of the gate pattern and a surface area of the gate pattern is enlarged; and

subsequently removing portions of the second insulating layer.

2. The method of forming a gate structure of claim 1, wherein said forming of the first insulating layer comprises forming an oxide layer on the substrate, and said coating the substrate with conductive material comprises forming a layer of polysilicon over the oxide layer.

3. The method of forming a gate structure of claim 1, wherein said forming of the second insulating layer comprises forming a low-temperature oxide

layer on the gate pattern.

4. The method of forming a gate structure of claim 3, wherein the low-temperature oxide layer is formed by a high-density plasma chemical vapor deposition (CVD) process.

5. The method of forming a gate structure of claim 4, wherein the low-temperature oxide layer is formed to a thickness of about 3000 Å.

6. The method of forming a gate structure of claim 1, wherein said removing some of the second insulating layer comprises planarizing the second insulating layer, and subsequently etching the second insulating layer.

7. The method of forming a gate structure of claim 6, wherein the planarizing of the second insulating layer comprises chemically mechanically polishing the second insulating layer until the upper surface thereof is situated about 700 Å over the upper surface of the gate pattern.

8. The method of forming a gate structure of claim 6, wherein said subsequent etching of the second insulating layer comprises wet etching the second insulating layer until the thickness thereof is about 900 Å.

9. The method of forming a gate structure of claim 8, wherein said wet etching of the second insulating layer is carried out using a limulus amoebocyte lysate (LAL) solution.

10. The method of forming a gate structure of claim 6, further comprising rinsing residuals of the second insulating layer, produced as a result of said etching thereof, before the second conductive layer is formed.

11. The method of forming a gate structure of claim 1, wherein the second conductive layer is formed to a thickness of about 300 Å to about 500 Å using a chemical vapor deposition (CVD) process.

12. The method of forming a gate structure of claim 1, wherein said removing of the second conductive layer comprises an anisotropic etching process.

13. The method of forming a gate structure of claim 12, wherein the removing portions of the second insulating layer is carried out using the spacer as a mask, so that the second insulating layer only remains at both sides of a lower portion of the gate pattern beneath the spacer.

14. The method of forming a gate structure of claim 13, further comprising forming a silicide layer on the gate pattern and the spacer.

15. A method of fabricating a semiconductor device, comprising:

forming a first insulating layer on a substrate, subsequently coating the substrate with a conductive material, and patterning the conductive material to form at least one gate pattern insulated from the substrate by the first insulating layer;

forming a second insulating layer on the gate pattern and the substrate;

removing some of the second insulating layer until an upper surface thereof is below a level of an upper surface of the gate pattern;

forming a second conductive layer comprising the conductive material on the second insulating layer and the gate pattern;

selectively removing portions of the second conductive layer such that the second insulating layer is exposed, so that a first spacer of the conductive material is formed at both sides of an upper portion of the gate pattern, and a surface area of the gate pattern is enlarged;

subsequently removing the second insulating layer except at portions adjacent both sides of a lower portion of the gate pattern;

subsequently implanting ions, at a relatively low concentration, into the substrate at both sides of the gate pattern using the gate pattern as a mask, to thereby form a lightly doped source/drain region on the substrate;

subsequently forming a fourth insulating layer on the substrate including the gate pattern;

selectively removing portions of the fourth insulating layer to thereby form a second spacer at the sides of the gate pattern;

subsequently implanting ions, at a concentration higher than that of said relatively low concentration, into the substrate corresponding at both sides of the gate pattern using the gate pattern and the second spacer as a mask, to thereby form a heavily doped source/drain region on the substrate;

subsequently performing a heat treatment on the substrate; and

forming a third conductive layer on the gate pattern and on the heavily-doped source/drain region.

16. The method of fabricating a semiconductor device of claim 15, wherein said forming of the first insulating layer comprises forming an oxide layer on the substrate, and said coating the substrate with conductive material comprises forming a layer of polysilicon over the oxide layer.

17. The method of fabricating a semiconductor device of claim 15, wherein said forming of the second insulating layer comprises forming a low-temperature oxide layer on the gate pattern.

18. The method of fabricating a semiconductor device of claim 15, wherein said removing the second insulating layer comprises planarizing the second insulating layer, and subsequently etching the second insulating layer.

19. The method of fabricating a semiconductor device of claim 18, wherein the second insulating layer is planarized by a chemical mechanical polishing process, and etched away through a wet etching process.

20. The method of fabricating a semiconductor device of claim 19, further comprising rinsing residuals of the second insulating layer, produced as a result of said etching thereof, before the second conductive layer is formed.

21. The method of fabricating a semiconductor device of claim 15, wherein the second conductive layer is formed to a thickness of about 300 Å to about 500 Å using a chemical vapor deposition (CVD) process, and said removing of the

second conductive layer comprises an anisotropic etching process.

22. The method of fabricating a semiconductor device of claim 21, wherein the second insulating layer etched by using the first spacer as a mask, so that the second insulating layer only remains at both sides of a lower portion of the gate pattern.

23. The method of fabricating a semiconductor device of claim 15, wherein portions of the first insulating layer are removed in said removing of the second insulating layer except at portions adjacent both sides of a lower portion of the gate pattern, whereby the surface of the substrate is exposed, and further comprising forming a third insulating layer on exposed portions of the substrate before the lightly-doped source/drain region is formed.

24. The method of fabricating a semiconductor device of claim 23, wherein said forming of the third insulating layer comprises forming an oxide layer on the exposed portions of the substrate using a CVD process or a physical vapor deposition (PVD) process

25. The method of fabricating a semiconductor device of claim 15, further comprising implanting anti-diffusion ions into the substrate at both sides of the gate pattern before said implanting of the ions at said relatively low concentration, to thereby prevent the subsequently implanted ions from diffusing to a region under the gate pattern.

26. The method of fabricating a semiconductor device of claim 25, wherein the anti-diffusion ions are selected from the group consisting of germanium (Ge), phosphor (P), silicon (Si) and indium (In) ions.

27. The method of fabricating a semiconductor device of claim 25, wherein the anti-diffusion ions are implanted into the substrate at both sides of the gate pattern at acute angles with respect to the upper surface of the substrate, respectively.

28. The method of fabricating a semiconductor device of claim 27, wherein the anti-diffusion ions are implanted into the substrate at a left side of the gate pattern at an angle in a range from about 30° to about 45° measured clockwise from the upper surface of the substrate, and are implanted into the substrate at a right side of the gate pattern at an angle in a range from about 30° to about 45° measured counter-clockwise from the upper surface of the substrate.

29. The method of fabricating a semiconductor device of claim 15, wherein said implanting of ions to form the lightly- and heavily- doped regions is carried out at an angle of about 90° with respect to the substrate.

30. The method of fabricating a semiconductor device of claim 15, wherein said forming of the another insulating layer on the substrate comprises forming a nitride layer using a CVD or a PVD process over the gate pattern.

31. The method of fabricating a semiconductor device of claim 15,

wherein said forming of the third conductive layer comprises forming a metal layer on the gate pattern and on the heavily-doped source/drain region, and subsequently heat-treating the substrate to produce a chemical reaction between the metal layer and the conductive material of the gate pattern.

32. A semiconductor device, comprising:

a semiconductor substrate, and an isolation structure, said semiconductor substrate having an active region defined by the isolation structure;

a gate insulating layer disposed on the active region of said substrate;

a gate electrode including

a gate electrode having a main body disposed on said gate insulating layer as in contact therewith, and wings extending laterally from an upper portion of said body, such that the gate electrode is T- or mushroom-shaped; and

a capacitance preventative layer of insulating material disposed under said wings of said gate electrode in contact with said body of the gate electrode and said gate insulating layer, and thereby limiting the parasitic capacitance that can be generated between the substrate and the gate electrode;

a spacer disposed both sides of said gate electrode, the spacer comprising an insulating material; and

a source electrode and a drain electrode located in the active region of said substrate, the source electrode and drain electrode being spaced apart from each other with said gate electrode being disposed therebetween.

33. The semiconductor device of claim 32, wherein said gate electrode comprises polysilicon, and said capacitance preventative layer comprises a low temperature oxide (LTO) layer.

34. The semiconductor device of claim 32, wherein said substrate has an anti-diffusion layer disposed beneath the gate insulating layer at both sides of the gate electrode, said anti-diffusion layer comprising anti-diffusion ions.

35. The semiconductor device of claim 34, wherein the anti-diffusion ions are selected from the group consisting of germanium (Ge), phosphor (P), silicon (Si) and indium (In) ions.

36. The semiconductor device of claim 32, wherein said gate electrode includes a layer comprising a metal at outer surfaces of said body and wings thereof.

37. The semiconductor device of claim 38, wherein the metal is selected from the group consisting of titanium (Ti), tungsten (W) and cobalt (Co).

38. The semiconductor device of claim 36, wherein a layer of said metal layer is also disposed on the source and drain electrodes.